UNIVERSITY COLLEGE TATI

UNIVERSITY COLLEGE TATI (UC TATI)

FINAL EXAMINATION QUESTION BOOKLET	
COURSE CODE	: BMT 2023
COURSE	: DIGITAL SYSTEM
SEMESTER/SESSION	: 2-2023/2024
DURATION	: 3 HOURS

Instructions:

1. This booklet contains **4** questions. Answer **ALL** questions.
2. All answers should be written in answer booklet.
3. Write legibly and draw sketches wherever required.
4. If in doubt, raise up your hands and ask the invigilator.

DO NOT OPEN THIS BOOKLET UNTIL YOU ARE TOLD TO DO SO

THIS BOOKLET CONTAINS 7 PRINTED PAGES INCLUDING COVER PAGE

QUESTION 1

a) List **THREE (3)** advantages of digital system. (3 marks)

b) List **TWO (2)** types of the number system used in the digital signal. (2 marks)

c) Describe **TWO (2)** differences between the analog signal and digital signal. (4 marks)

d) Convert the hexadecimal number of 55.4_{16} to octal number. Shows the working method. (8 marks)

e) Convert the decimal number, 453.42_{10} to binary coded decimal (BCD) number. Shows the working method. (5 marks)

f) Refer to Figure 1. Complete the output timing diagram, Z in Figure 2 with A and B as the input signal. (4 marks)

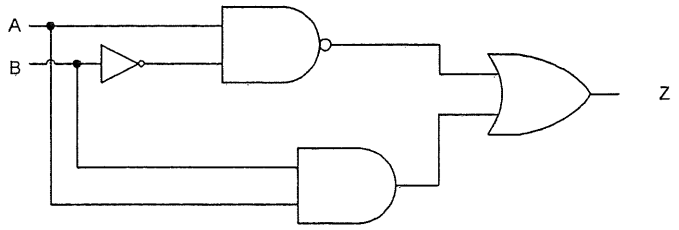

Figure 1

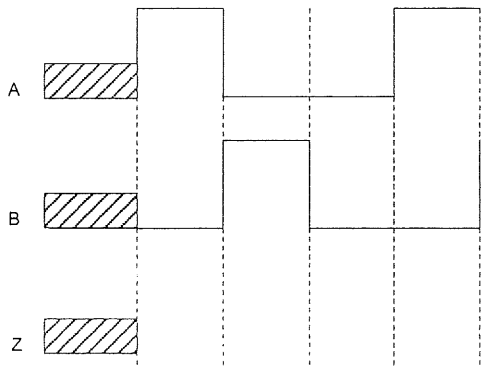

Figure 2

QUESTION 2

a) List **THREE (3)** types of logic gates. (3 marks)

b) Produce the simplified standard sum-of-products (SOP) expression for the K-map shown in Figure 3. (6 marks)

AB \ CD	00	01	11	10
00	1	1	1	1
01	0	0	1	0
11	0	0	0	1
10	1	0	0	1

Figure 3

c) Refer to the full adder shown in Figure 4.

i. Develop a 4-bit adder using the full adder. (4 marks)

ii. Shows the logic state of each input and output if $X=1101_2$ and $Y=1110_2$. (4 marks)

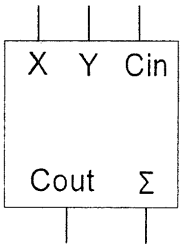

Figure 4

d) Develop the Boolean expression of $F(A,B,C) = \sum m(1,2,3,4,7)$ using 4-to-1 multiplexer. (10 marks)

QUESTION 3

a) List **THREE (3)** examples of combinational logic circuit. (3 marks)

b) For the Boolean expression below.

$$F(A,B,C,D) = ABC + \bar{A}BC + ACD + BCD$$

i. Produce the standard sum-of-products (SOP) expression. (4 marks)

ii. Simplify the standard SOP output expression using K-Map. (5 marks)

c) Refer to Figure 5. Determine the output timing diagram, Q in Figure 6 assuming that the flip-flop is initially RESET. (5 marks)

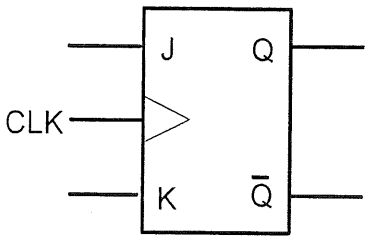

Figure 5

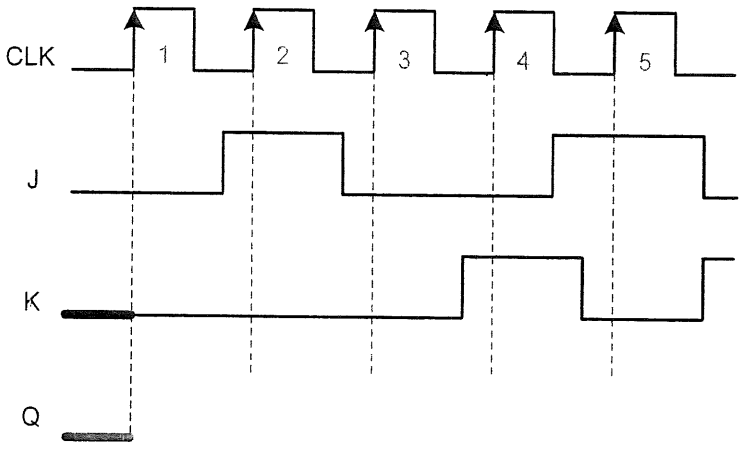

Figure 6

d) Refer to Figure 7. Determine the output waveforms in relation to the clock for Q_A, Q_B, and Q_C in Figure 8 assuming the initial output is 0. (9 marks)

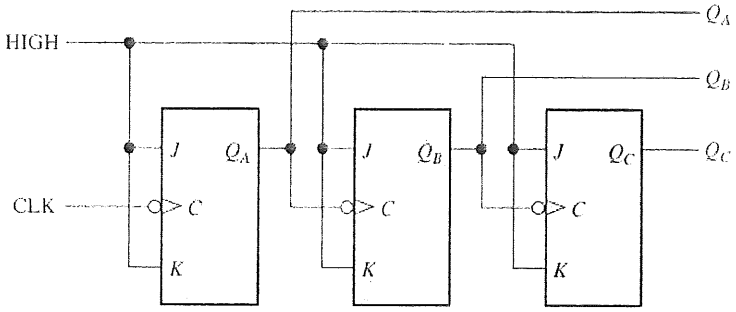

Figure 7

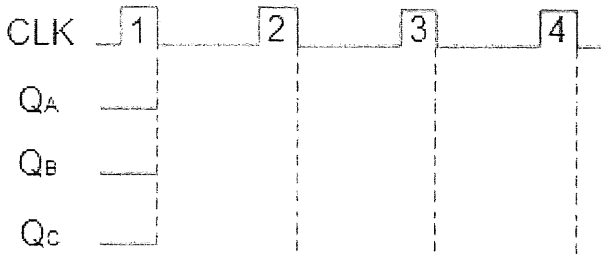

Figure 8

QUESTION 4

a) List **THREE (3)** types of shift register. (3 marks)

b) Develop a 4-bit ring counter using D flip-flop. (4 marks)

c) A synchronous counter with a counting sequence as shown in Figure 9 is designed by using JK flip-flops. Assume all unused states are forced to don't care condition.

i. Determine the next state and the input of J_A, K_A, J_B, K_B, J_C and K_C as listed in Table 1. (5 marks)

ii. Simplify the Boolean equation for J_A, K_A, J_B, K_B, J_C and K_C by using K-map. (6 marks)

iii. Draw logic circuit based on the simplified Boolean expression obtained in question 4c(ii) using positive edge triggered JK flip-flop circuit with active high clock and other suitable logic gates. (3 marks)

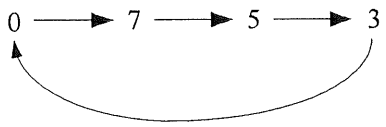

Figure 9

Table 1

PRESENT STATE	NEXT STATE						
A B C	A' B' C'	J_A	K_A	J_B	K_B	J_C	K_C
0 0 0							
0 0 1							
0 1 0							
0 1 1							
1 0 0							
1 0 1							
1 1 0							
1 1 1							

----------End of Question----------

APPENDIX 1

Table 1: Rules of Boolean Algebra

1. $A + 0 = A$	7. $A \cdot A = A$
2. $A + 1 = 1$	8. $A \cdot \overline{A} = 0$
3. $A \cdot 0 = 0$	9. $\overline{\overline{A}} = A$
4. $A \cdot 1 = A$	10. $A + AB = A$
5. $A + A = A$	11. $A + \overline{A}B = A + B$
6. $A + \overline{A} = 1$	12. $(A + B)(A + C) = A + BC$

Table 2: Excitation Table

Flip-Flop Name	Excitation Table
SR	Q_n Q_{n+1} S R 0 0 0 X 0 1 1 0 1 0 0 1 1 1 X 0
JK	Q_n Q_{n+1} J K 0 0 0 X 0 1 1 X 1 0 X 1 1 1 X 0
D	Q_n Q_{n+1} D 0 0 0 0 1 1 1 0 0 1 1 1
T	Q_n Q_{n+1} T 0 0 0 0 1 1 1 0 1 1 1 0